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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/768,665	01/24/2001	Tuyet-Huong Thi Nguyen	016295.0624	3786

7590 10/06/2005

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EXAMINER	
KING, JUSTIN	

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 10/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/768,665	NGUYEN ET AL.	
	Examiner	Art Unit	
	Justin I. King	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 8/8/05.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1,4-8,16 and 19-23 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1,4-8,16 and 19-23 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 1, 4-8, 16, and 19-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art in view of Goodman et al. (U.S. Patent No. 6,282,601) and Smith et al. (U.S. Patent No. 3,643,227).

Referring to claim 1: The admitted prior art discloses writing parameters for the SMI routines to a predetermined register of a first processor (Specification, page 3, lines 4-6), executing in the first processor a command of a software application to cause the first processor to initiate a system management interrupt (Specification, page 2, lines 8-17), receiving at each processor an instruction that the system management interrupt has been issued (Specification, page 2, lines 19-20), entering system management mode at each processor (Specification, page 2,

lines 20-21), and saving register contents of each processor to a memory space associated with each respective processor (Specification, page 2, lines 22-24). The admitted prior art's parameters for the SMI routines are the claimed predetermined signature.

The admitted prior art further discloses that a different processor, other than the processor initiating the interrupt, may be selected for handling the interrupt (Specification, page 3, lines 13-16); thus, the admitted prior art discloses selecting from among the multiple processors a second processor as a system management interrupt handler.

But the admitted prior art does not disclose selecting the second processor according to an arbitration scheme. The admitted prior art also does not disclose scanning the content of the memory for the selected second processor to process the interrupt.

Goodman discloses an interrupt handling method in a multiprocessor environment. Goodman discloses scanning the contents of the memory space associated with each processor (figure 4, steps 126, 128, and 130); and when the second processor locates the saved predetermined signature in one of the memory spaces associated with the processors of the computers system, using the contents of the memory space associated with the predetermined signature for any parameters necessary for the handling of the system management interrupt (figure 4, steps 134, 136, and 138). Goodman teaches one to identify the requesting processor without having to satisfy severe interrupt timing constraint (column 1, lines 66-67, column 2, lines 1-5). Although Goodman discloses and teaches one to select a processor to handle the interrupt, Goodman does not explicitly disclose an arbitration scheme in selecting the processor.

Smith discloses assigning tasks to the idle processor (abstract). Smith teaches one to distribute the task to the processor based on the processor's current workload.

Hence, it would have been obvious to one having ordinary skill in the computer art to adapt the teachings of Goodman and Smith onto the admitted prior art because Goodman teaches one to identify the requesting processor without having to satisfy severe interrupt timing constraint and Smith teaches one to balance each processor's workload by distributing the task according to the processor's current workload

Referring to claim 4: Claim 1's argument applies; furthermore, since Smith teaches one to select the processor based on the workload; it can be any processor, including the one just causes the SMI.

Referring to claim 5: The admitted prior art discloses the processors' access to chip set's I/O port as one standard well-known system activities (Application, page 3, lines 8-9). Goodman also discloses that the processor writes to the memory (figure 1, structure 26) via the chip set's port (figure 1, structure 18).

Referring to claims 6-7: Both the admitted prior art (Specification, page 2, line 11) and Goodman (figure 1, structure 50) disclose the chip sets as a PCI bridge.

Referring to claim 8: The admitted prior art discloses the step of issuing from the expansion bridge the instruction causing the processor to enter the system management mode (Specification, page 2, lines 10-17). Goodman discloses that each of the processors of the system to enter system management mode (column 1, lines 50-54).

Referring to claim 16: The admitted prior art discloses issuing an instruction from a first processor of the system to a chip set (Specification, page 2, lines 10-11), receiving the instruction at the chip set and in response issuing a command causing the processors to enter system management mode (Specification, page 2, lines 12 and 18-19), writing parameters for the SMI

routines to a predetermined register of a first processor (Specification, page 3, lines 4-6), and saving register contents of each processor to a memory space associated with each respective processor (Specification, page 2, lines 22-24). The admitted prior art's parameters for the SMI routines are the claimed predetermined signature.

The admitted prior art further discloses that a different processor, other than the processor initiating the interrupt, may be selected for handling the interrupt (Specification, page 3, lines 13-16); thus, the admitted prior art discloses selecting from among the multiple processors a second processor as a system management interrupt handler and then transmitting the software system management interrupt to the selected second processor.

But the admitted prior art does not disclose selecting the second processor according to an arbitration scheme. The admitted prior art also does not disclose retrieving the content of the memory for the selected second processor to process the interrupt.

Goodman discloses an interrupt handling method in a multiprocessor environment. Goodman discloses scanning the contents of the memory space associated with each processor (figure 4, steps 126, 128, and 130); and when the second processor locates the saved predetermined signature in one of the memory spaces associated with the processors of the computers system, using the contents of the memory space associated with the predetermined signature for any parameters necessary for the handling of the system management interrupt (figure 4, steps 134, 136, and 138). Goodman teaches one to identify the requesting processor without having to satisfy severe interrupt timing constraint (column 1, lines 66-67, column 2, lines 1-5). Although Goodman discloses and teaches one to select a processor to handle the interrupt, Goodman does not explicitly disclose an arbitration scheme in selecting the processor.

Smith discloses assigning tasks to the idle processor (abstract). Smith teaches one to distribute the task to the processor based on the processor's current workload.

Hence, it would have been obvious to one having ordinary skill in the computer art to adapt the teachings of Goodman and Smith onto the admitted prior art because Goodman teaches one to identify the requesting processor without having to satisfy severe interrupt timing constraint and Smith teaches one to balance each processor's workload by distributing the task according to the processor's current workload.

Referring to claim 19: The admitted prior art discloses the processors' access to chip set's I/O port as one standard well-known system activities (Application, page 3, lines 8-9). Goodman also discloses that the processor writes to the memory (figure 1, structure 26) via the chip set's port (figure 1, structure 18).

Referring to claims 20-21: Both the admitted prior art (Specification, page 2, line 11) and Goodman (figure 1, structure 50) disclose the chip sets as a PCI bridge.

Referring to claims 22-23: The admitted prior art discloses receiving at each processor an instruction that the system management interrupt has been issued (Specification, page 2, lines 19-20) and entering system management mode at each processor (Specification, page 2, lines 20-21).

The admitted prior art further discloses that a different processor, other than the processor initiating the interrupt, may be selected for handling the interrupt (Specification, page 3, lines 13-16); thus, the admitted prior art discloses selecting from among the multiple processors a second processor as a system management interrupt handler.

But the admitted prior art does not disclose selecting the second processor according to an arbitration scheme. The admitted prior art also does not disclose scanning, locating, and retrieving the content of the memory for the selected second processor to process the interrupt.

Goodman discloses an interrupt handling method in a multiprocessor environment. Goodman discloses scanning the contents of the memory space associated with each processor (figure 4, steps 126, 128, and 130); and when the second processor locates the saved predetermined signature in one of the memory spaces associated with the processors of the computers system, using the contents of the memory space associated with the predetermined signature for any parameters necessary for the handling of the system management interrupt (figure 4, steps 134, 136, and 138). Goodman teaches one to identify the requesting processor without having to satisfy severe interrupt timing constraint (column 1, lines 66-67, column 2, lines 1-5). Although Goodman discloses and teaches one to select a processor to handle the interrupt, Goodman does not explicitly disclose an arbitration scheme in selecting the processor.

Smith discloses assigning tasks to the idle processor (abstract). Smith teaches one to distribute the task to the processor based on the processor's current workload.

Hence, it would have been obvious to one having ordinary skill in the computer art to adapt the teachings of Goodman and Smith onto the admitted prior art because Goodman teaches one to identify the requesting processor without having to satisfy severe interrupt timing constraint and Smith teaches one to balance each processor's workload by distributing the task according to the processor's current workload.

Response to Arguments

4. In response to Applicant's arguments that Goodman does not disclose or teach a selection among the multiple processors operable to handle the system interrupt management (Remark, page 9, 4th paragraph), and Applicant further argues that Goodman discloses only the boot processor handles the interrupt management (Remark, page 9, 4th paragraph): As Applicant stated, Goodman discloses dedicating the boot processor to handle the interrupt management; the practice of Goodman's dedicating one processor to handle the interrupt management is the claimed selecting means. Also as Applicant stated, in Goodman, only the boot processor handles the system interrupt management, which is because that this processor is selected to handle the interrupt management.

5. In response to Applicant's argument that Goodman teaches away from the claimed invention because Goodman discloses that all system management interrupts are to be handled by a single dedicated processor (Remark, page 10, 2nd paragraph): Goodman discloses and teaches one to select a processor to handle the interrupt at any given time, but Goodman does not explicitly disclose an arbitration scheme in selecting the processor. Smith discloses assigning tasks to the idle processor (abstract). Smith teaches one to distribute the task to the processor based on the processor's current workload.

6. In response to Applicant's argument that Goodman does not suggest any processor other than the boot processor is operable to handle the management interrupt, and a plain reading of the Goodman would lead a person of ordinary skill to conclude that only a single dedicated processor may be designed as the processor for handling management interrupt, and nowhere Goodman suggests that multiple processors could be used to handle management interrupts

(Remark, page 10, 3rd paragraph), thus Goodman teaches away from the alleged invention (Remark, page 10, last paragraph): One with ordinary skill in the computer art would know that any processor is operable to handle management interrupt. The plain reading of the Goodman does not lead a person of ordinary skill in the computer art to conclude that **only** a single dedicated processor may be designed as the processor for handling management interrupt. Goodman discloses that it is known to have a dedicated interrupt processor, and Goodman discloses the practice of selecting the boot processor as stated by the Applicant, but Goodman does not disclose that only this processor is capable of handling interrupt management.

7. In response to Applicant's argument that Examiner recognizes that Goodman teaches away (Remark, page 11, 1st paragraph): Applicant merely alleged Examiner's recognition without quoting any portion from the previous Office Action.

8. In response to Applicant's argument that it is well established that each prior art must be considered in its entirety; thus, Goodman must be considered in its entirety, Applicant quoted W.L. Gore & Assoc., Inc. v. Garlock, Inc., In re Hedges, Smith Kline Diagnostics, Inc. v. Helena Laboratories Corp., and Johnson & Son, Inc. (Remark, page 11, last 2 paragraph, pages 12-13): There is no such establishment, as alleged, to consider every prior art on record in its entirety. Applicant should provide appropriate MPEP section to support the alleged establishment, and Applicant should also point out and quote the appropriate section in the judicial opinion to support the alleged establishment and reason why it is applicable in the instant case.

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Justin I. King whose telephone number is 571-272-36283628. The examiner can normally be reached on max flex. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3632 or on the central telephone number, (571) 272-2100. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lastly, paper copies of cited U.S. patents and U.S. patent application publications will cease to be mailed to applicants with Office actions as of June 2004. Paper copies of foreign patents and non-patent literature will continue to be included with office actions. These cited U.S. patents and patent application publications are available for download via the Office's PAIR. As an alternate source, all U.S. patents and patent application publications are available on the USPTO web site (www.uspto.gov), from the Office of Public Records and from commercial sources. Applicants are referred to the Electronic Business Center (EBC) at http://www.uspto.gov/ebc/index.html or 1-866-217-9197 for information on this policy. Requests to restart a period for response due to a missing U.S. patent or patent application publications will not be granted.

Justin King
September 29, 2005

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